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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,292	09/19/2003	KOHJI HOSOKAWA	JP920020166US1	2291

32074 7590 11/01/2004

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EXAMINER
TRAN, MICHAEL THANH

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,292	HOSOKAWA ET AL.	
	Examiner	Art Unit	
	Michael t Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *September 19, 2003-October 24, 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15-18* is/are allowed.

6)☒ Claim(s) *1-9,11,12 and 14* is/are rejected.

7)☒ Claim(s) *10 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *102403*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the Communications dated September 19, 2003 through October 24, 2003, claims 1-18 are active in this application.

Information Disclosure Statement

2. The information disclosure statement filed October 24, 2003 has been considered.

Claim Objections

3. Claims 10 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections – 35 U.S.C. § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

5. Claims 1-6 are rejected under 35 U.S.C 102(b) as being anticipated by Takeuchi et al. [U.S. Patent #6,046,940].

With respect to claim 1, Takeuchi et al. disclose, in figure 22, a dram circuit comprising a plurality of aligned sense amplifiers [SAO-SA3], bit line pairs [BL0, /BLO, BL1, /BL1, etc.] connected to the plurality of sense amplifiers, respectively, and memory cells [MCs] connected respectively to the bit lines constituting the bit line pairs, wherein the bit line pairs and the memory cells are alternately arranged on a right side [upper side] and a left side [lower side] of the sense amplifiers per N [N:natural number] aligned sense amplifiers.

With respect to claim 2, Takeuchi et al. further disclose, in figure 22, that there cross two bit lines constituting the bit line pair arranged on one side of a right side [upper side] and a left side [lower side] of the sense amplifier, and a space between the bit lines widens or narrows from the cross.

With respect to claim 3, Takeuchi et al. further disclose, in figure 22, that the two bit lines constituting the bit line pair, which is arranged on the other side of the one right side [upper side] or left side [lower side] of the sense amplifier, do not cross, and a space therebetween widens or narrows on the way.

With respect to claim 4, Takeuchi et al. further disclose, in figure 22, that the bit line pairs arranged on one of the right side [upper side] and left side [lower side] of the

sense amplifier are both connected to corresponding data lines [I/O] via bit switches [CSL0-N].

With respect to claim 5, Takeuchi et al. further disclose, in figures 22 and 33, that the plurality of aligned sense amplifiers is divided every M sense amplifiers [M: natural number], and a set driver is disposed in a separated area [column/row decoders]. It is noted that the array of sense amplifiers can be interpreted as a plurality of sub-arrays [divided arrays].

With respect to claim 6, Takeuchi et al. further disclose, that there exists multiple twisted sections of the plurality of bit line pairs. See figure 23.

6. Claim 7 is rejected under 35 U.S.C 102(b) as being anticipated by Takeuchi et al. [U.S. Patent #6,046,940].

With respect to claim 7, Takeuchi et al. disclose, in figure 22, a dram circuit comprising: a plurality of sense amplifiers [for example 4] arranged in Q lines [4 lines] each containing the P sense amplifiers [figure 22 only shows a portion of the entire memory array]; bit line pairs connected to the plurality of sense amplifiers, respectively; and memory cells connected respectively to the bit lines constituting the bit line pairs, wherein the bit line pairs and the memory cells arranged every N [N: natural number] aligned sense amplifiers in the Q lines [4 lines], alternately on a right side [upper side] and a left side [lower side] of the sense amplifiers, and P and Q are both integers of more than 3 [in this case, Takeuchi et al. show more than 3], and N is an arbitary integer of more than 1 and less than [P/3] [in this case, Takeuchi et al. show more than 1].

7. Claims 8, 9, 11, and 12 are rejected under 35 U.S.C 102(b) as being anticipated by Ong et al. [U.S. Patent #5,999,480].

With respect to claim 8, Ong et al. disclose, in figure 22, a dram circuit comprising a plurality of sense amplifiers SA[J,K] arranged in Q lines each containing the P sense amplifiers, bit lines pairs connected to the plurality of sense amplifiers SA [J,K], respectively, and memory cells [MCs] connected respectively to the bit lines constituting the bit line pairs, wherein the sense amplifier SA [J,K] is connected to each of the bit line pairs arranged between the sense amplifier SA [J,K] and a sense amplifier SA [J, K-1] in one next line or a sense amplifier SA[J,K+1] is connected to the bit line pairs arranged between the sense amplifier SA [J+1, K] and a sense amplifier SA [J+1, K+1] in one next line or a sense amplifier SA [J+1, K-1] in the other next line; a sense amplifier SA [J+3,k] is connected to each of the bit line pairs arranged between the sense amplifier SA [J+3,K] and a sense amplifier SA [J+2, k-1] in one next line or a sense amplifier SA [J+2, K+1] in the other next line [in this case, assuming that the second row SA on the left hand side of figure 14 is SA [J,K] – it is noted that with this assumption, Ong et al. disclose only a portion of the array with regard to figure 14]; and P and Q are both integers of more than 3, J is an arbitrary integer of more than 1 and less than P, and K is an arbitrary integer of more than 1 and less than Q. In this case, Ong et al. disclose, in figure 14, that there exists more than 3 sense amplifiers arranged on more than 3 lines. Ong et al. also disclose that there are more than 1 memory cells.

With respect to claim 9, Ong et al. disclose that the bit line pairs arranged between one sense amplifier and the next cross [see figure 14] and from the cross, the space between the bit lines widens.

With respect to claim 11, Ong et al. disclose, in figure 14, that the bit line pairs are connected to corresponding data lines [I/O] via bit switches [transistors coupled to the sense amplifiers].

With respect to claim 12, Ong et al. disclose, in figure 14, that the sense amplifiers [the array can be interpreted as have a plurality of sub-arrays], whose number arranged in one line P, is divided every M sense amplifiers, and a set driver [row/column circuitry] is disposed in a separated area.

8. Claims 14 are rejected under 35 U.S.C 102(b) as being anticipated by Ong et al. [U.S. Patent #5,999,480].

With respect to claim 14, Ong et al. disclose, in figure 14, a DRAM circuit comprising: a plurality of sense amplifiers SA(J, K) arranged in Q lines each containing the P sense amplifiers; bit line pairs connected to the plurality of sense amplifiers SA(J, K), respectively, and memory cells connected respectively to the bit lines constituting the bit line pairs, wherein the sense amplifier SA(J, K) and a sense amplifier SA(J+1, K) are each connected to each of the bit line pairs arranged between a sense amplifier SA (J, K-1) in one next line and a sense amplifier SA between a sense amplifier SA(J+1, K-1) or between (J, K+ 1) in the other next line and a sense amplifier SA (J+1, K+ 1)., a sense amplifier SA (J+2, K) and a sense amplifier SA (J+3, K) are each connected to the bit line pairs arranged between a sense amplifier SA (J+2, K+ 1) in one next line

and a sense amplifier SA (J+3, K+ 1) or between a sense amplifier SA (J+2, K-1) in the other next line and a sense amplifier SA (J+3, K- 1), a sense amplifier SA (J+4, K) and a sense amplifier SA (J+5, K) are each connected to each of the bit line pairs arranged between a sense amplifier SA (J+4, K-1) in one next line and a sense amplifier SA (J+5, K-1) or between a sense amplifier SA (J+4, K+ 1) in the other next line and a sense amplifier SA (J+4, K+ 1), and P and Q are both integers of more than 6, J is an arbitrary integer of more than 1 and less than P, and K is an arbitrary integer of more than 1 and less than Q. In this case, assuming that the second row SA on the left hand side of figure 14 is SA [J,K] – it is noted that with this assumption, Ong et al. disclose only a portion of the array with regard to figure 14. Also, Ong et al. disclose, in figure 14, that there exists more than 3 sense amplifiers arranged on more than 3 lines. Ong et al. also disclose that there are more than 1 memory cells.

Allowable Subject Matter

9. Claims 15-18 are allowable over the prior art of record.

10. The following is an Examiner's statement of reasons for the indication of allowable subject matter: the prior art of records does not show (in addition to the other elements in the claim) the following:

- A step of activating the plurality of sense amplifiers connected to the bit line pairs and memory cells arranged on the right side [upper side] of the sense amplifiers, and the plurality of sense amplifiers connected to the bit line pairs and memory

cells arranged on the left side [lower side] of the sense amplifiers at different timing, when data is read.

Conclusion

11. When responding to the Office action, Applicants are advised to provide the Examiner with line and page numbers of the application and/or references cited to assist the Examiner in the prosecution of this case.

12. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Michael T. Tran whose telephone number is (571) 272-1795. The Examiner can normally be reached on Monday-Thursday from 7:30-6:00 P.M.

13. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-1650.

Michael T. Tran
Art Unit 2818
October 29, 2004